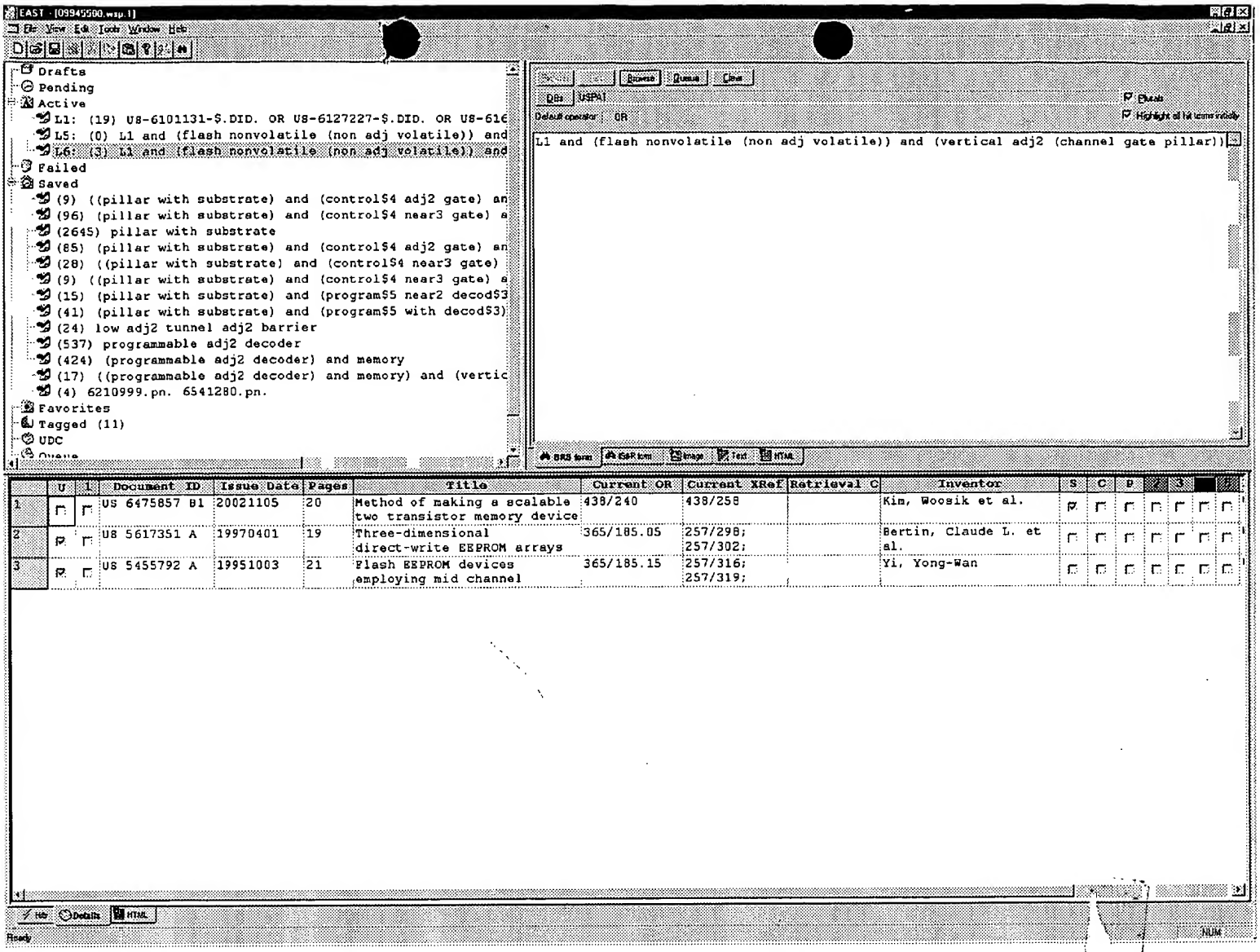
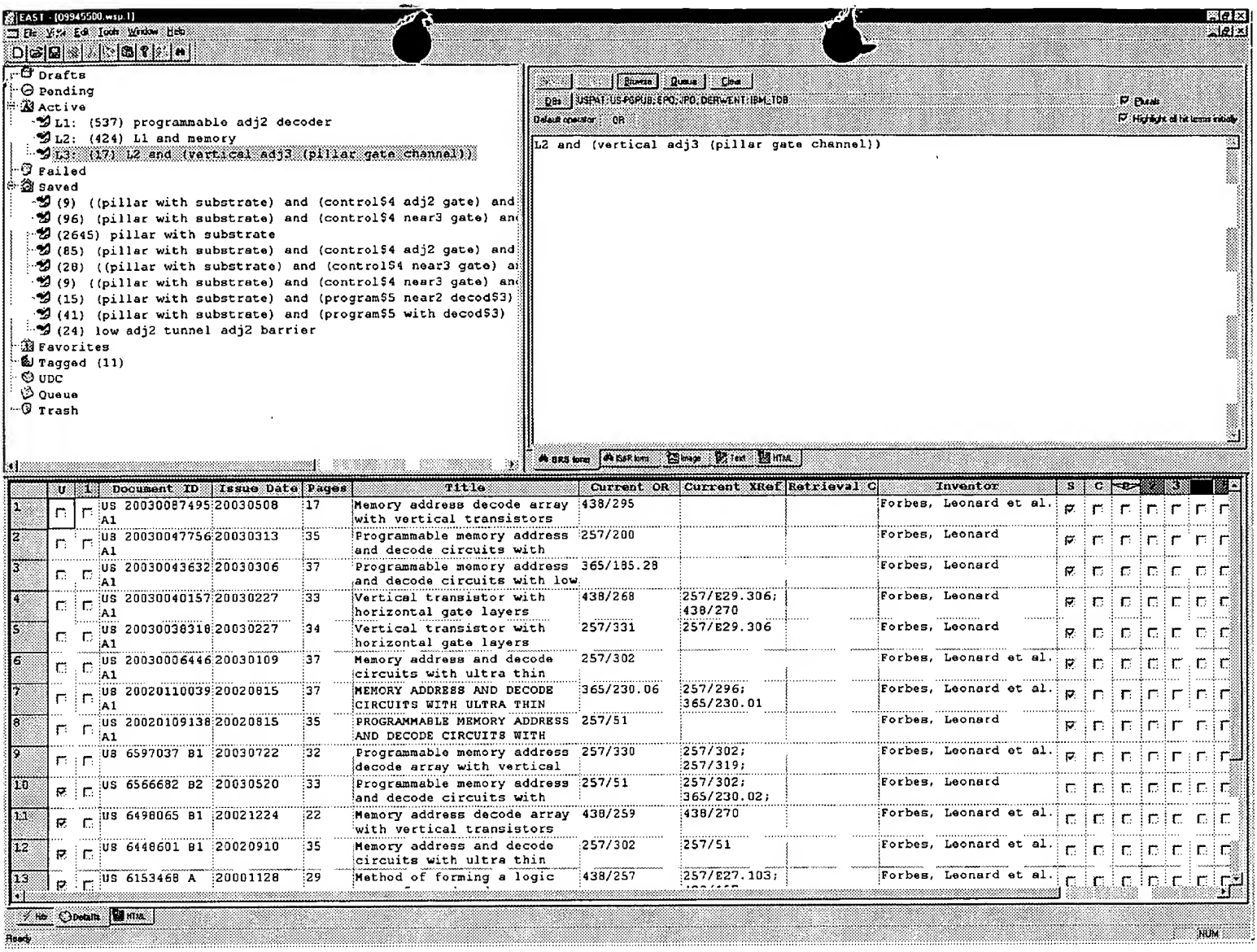


	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	P	2	3		#:
1	☐	☐	US 6475857 B1	20021105	20	Method of making a scalable two transistor memory device	438/240	438/258		Kim, Woosik et al.	☑	☐	☐	☐	☐	☐	☐
2	☑	☐	US 5617351 A	19970401	19	Three-dimensional direct-write EEPROM arrays	365/185.05	257/298; 257/302;		Bertin, Claude L. et al.	☐	☐	☐	☐	☐	☐	☐
3	☑	☐	US 5455792 A	19951003	21	Flash EEPROM devices employing mid channel	365/185.15	257/316; 257/319;		Yi, Yong-Wan	☐	☐	☐	☐	☐	☐	☐



	U	L	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	C	2	3
1			US 20030087495 A1	20030508	17	Memory address decode array with vertical transistors	438/295			Forbes, Leonard et al.	☑			
2			US 20030047756 A1	20030313	35	Programmable memory address and decode circuits with	257/200			Forbes, Leonard	☑			
3			US 20030043632 A1	20030306	37	Programmable memory address and decode circuits with low	365/185.28			Forbes, Leonard	☑			
4			US 20030040157 A1	20030227	33	Vertical transistor with horizontal gate layers	438/268	257/E29.306; 438/270		Forbes, Leonard	☑			
5			US 20030036310 A1	20030227	34	Vertical transistor with horizontal gate layers	257/331	257/E29.306		Forbes, Leonard	☑			
6			US 20030006446 A1	20030109	37	Memory address and decode circuits with ultra thin	257/302			Forbes, Leonard et al.	☑			
7			US 20020110039 A1	20020815	37	MEMORY ADDRESS AND DECODE CIRCUITS WITH ULTRA THIN	365/230.06	257/296; 365/230.01		Forbes, Leonard et al.	☑			
8			US 20020109138 A1	20020815	35	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH	257/51			Forbes, Leonard	☑			
9			US 6597037 B1	20030722	32	Programmable memory address decode array with vertical	257/330	257/302; 257/319;		Forbes, Leonard et al.	☑			
10	☑		US 6566682 B2	20030520	33	Programmable memory address and decode circuits with	257/51	257/302; 365/230.02;		Forbes, Leonard				
11	☑		US 6498065 B1	20021224	22	Memory address decode array with vertical transistors	438/259	438/270		Forbes, Leonard et al.				
12	☑		US 6448601 B1	20020910	35	Memory address and decode circuits with ultra thin	257/302	257/51		Forbes, Leonard et al.				
13	☑		US 6153468 A	20001128	29	Method of forming a logic	438/257	257/E27.103;		Forbes, Leonard et al.				

L Number	Hits	Search Text	DB	Time stamp
1	537	programmable adj2 decoder	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/11 13:56
2	424	(programmable adj2 decoder) and memory	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/11 13:56
3	17	((programmable adj2 decoder) and memory) and (vertical adj3 (pillar gate channel))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/11 13:57